REMARKS

In the Office Action, the Examiner rejected claims 1-3, 6-12, 15, 16, 18, and 19 under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent No. 6,800,885 to An et al. ("An") in view of U.S. Patent No. 5,663,586 to Lin ("Lin"); rejected claims 1-3, 6, 7, 16, 18, and 19 under 35 U.S.C. § 103(a) as being unpatentable in view of U.S. Patent No. 6,657,252 to Fried et al. ("Fried") in view of Lin; rejected claims 4 and 13 under 35 U.S.C. § 103(a) as being unpatentable over An and Lin and further in view of U.S. Patent No. 6,787,476 to Dakshina-Murthy et al. ("Dakshina-Murthy"); and rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Fried, Lin, and Dakshina-Murthy.

By this Amendment, Applicants amend claims 1 and 16 to define that the gate (claim 1) or gate material layer (claim 16) is in contact with the first and second sidewall spacers.

Applicants submit that the rejections of the claims under 35 U.S.C. § 103(a) that include the An patent are respectfully traversed, as An does not qualify as prior art under 35 U.S.C. § 103(a). Specifically, the rejection of claims 1-3, 6-12, 15, 16, 18, and 19 under 35 U.S.C. § 103(a) based on An and Lin and the rejection of claims 4 and 13 under 35 U.S.C. § 103(a) based on An, Lin, and Dakshina-Murthy are respectfully traversed. U.S.C. § 103(c) qualifies 35 U.S.C. § 103(a) and states:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

(35 U.S.C. § 103(c)). An qualifies as prior art under 35 U.S.C. § 102 only under subsection (e), and An and the pending application are both assigned to Advanced Micro Devices, Inc. Accordingly, An is not available to preclude patentability under 35 U.S.C. § 103(a).

The above arguments relating to An not being available as a prior art reference under 35 U.S.C. § 103(a) were made in the previous Amendment. In the Office Action, the Examiner contends that Applicants' statement that both An and the pending application are commonly assigned is not sufficient to remove An as an available prior art reference. The Examiner cited MPEP 706.02(l)(2) for support. This section of the MPEP states, in pertinent part:

> In order to be disqualified as prior art under 35 U.S.C. 103(c), the subject matter which would otherwise be prior art to the claimed invention and the claimed invention must be commonly owned at the time the claimed invention was made or subject to an obligation of assignment that would establish common ownership.

(MPEP 706.02(l)(2)). In further support of Applicants' contention that An is not available as a prior art reference, Applicants note that the Assignment document for the current application was signed in April and May of 2003, which is before the filing date of the current application. The Assignment was recorded at Reel 014466, Frame 0691. Also, Applicants attach a printout of the patent office's PAIR system for the Assignment document filed in the An patent application. As shown, this Assignment was signed by both inventors and was executed on February 6, 2003, also before the filing date of the current application. Accordingly, Applicants submit that the subject matter of the currently claimed invention and the subject matter of the An patent were commonly owned at the time of the current invention. Thus, the rejections under 35 U.S.C. § 103(a) that include An are improper and should be withdrawn.

Additionally, Applicants submit that the rejections of the claims under 35 U.S.C. § 103(a) that include the Dakshina-Murthy patent are respectfully traversed, as Dakshina-Murthy does not qualify as prior art under 35 U.S.C. § 103(a). Specifically, the rejection of claims 4 and 13 under 35 U.S.C. § 103(a) as being unpatentable over An, Lin, and Dakshina-Murthy, and the rejection of claim 4 as being unpatentable over Fried, Lin, and Dakshina-Murthy, are respectively

traversed on the grounds that Dakshina-Murthy is not available as a prior art reference.

Dakshina-Murthy is not available to preclude patentability under 35 U.S.C. § 103(a) for reasons similar to those given above regarding An. Applicants attach a printout of the patent office's PAIR system for the Assignment document filed in the Dakshina-Murthy patent application. As shown, this Assignment was signed by all inventors and was executed on December 13, 2002 and January 10, 2003, both before the filing date of the current application. Accordingly, Applicants submit that the subject matter of the currently claimed invention and the subject matter of the Dakshina-Murthy patent were commonly owned at the time of the current invention. Thus, the rejections under 35 U.S.C. § 103(a) that include Dakshina-Murthy are improper and should be withdrawn.

Claims 1-3, 6, 7, 16, 18, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fried in view of Lin. Applicants respectfully traverse this rejection.

Claim 1, as amended, is directed to a semiconductor device comprising, among other things, a first sidewall spacer formed adjacent a first side of a fin, the first sidewall spacer having a substantially triangular shaped cross-section; a second sidewall spacer formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and a gate formed over the fin and the first and second sidewall spacers, and in contact with the first and second sidewall spacers, in a channel region of the semiconductor device. The first and second sidewall spacers are formed to a width ranging from about 150 Å to about 1000 Å.

Applicants submit that Fried and Lin, either alone or in combination, do not disclose each of the features recited in claim 1, as amended. Claim 1, for instance, recites a gate formed over the fin and the first and second sidewall spacers, and in contact with the first and second sidewall

spacers, in a channel region of the semiconductor device.

Fried does not disclose or suggest the gate recited in claim 1. The Examiner contends that floating gates 115 of Fried correspond to Applicants' claimed first and second sidewall spacers and that gate 120 of Fried corresponds to Applicants' claimed gate. (Office Action, page 7). As clearly shown and described by Fried, a floating gate isolation layer 116 is disposed between layers 115 and 120 of Fried. (See Fried, Figs. 8, 10, and 11, and column 5, line 39 through column 6, line 11). Thus, floating gates 115 of Fried cannot be said to be in contact with gate 120 of Fried. Accordingly, Fried does not disclose or suggest, as is recited in claim 1, a gate formed over a fin and first and second sidewall spacers, and in contact with the first and second sidewall spacers.

Applicants have reviewed Lin, and submit that Lin also fails to remedy the deficiencies of Fried with respect to claim 1.

For at least these reasons, Applicants submit that Fried and Lin, either alone or in combination, do not disclose or suggest each feature of claim 1.

Additionally, Applicants submit that the Examiner has not shown proper motivation to combine Fried and Lin in the manner suggested. The Examiner relies on Lin for the width of the sidewall spacers recited in claim 1, and states that "[I]t would have been obvious to one skilled in this art to form Fried's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick." (Office Action, page 8). Applicants respectfully disagree with the Examiner's conclusion of obviousness. Fried discloses a FinFET CMOS device in which a fin extends vertically from the substrate of the device. (Fried, Title and column 2, lines 43-47). Lin discloses a more conventional FET device. (Lin, Title and Abstract). Applicants submit that these two structures

would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device. Accordingly, one of ordinary skill in the art reading Lin would not be motivated to use the spacer width disclosed by Lin as the width of the floating gate disclosed by Fried. Thus, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Fried and Lin.

For at least these reasons, Applicants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Fried and Lin is improper and should be withdrawn. At least by virtue of their dependency on claim 1, the rejection of claims 2, 3, 6, and 7 based on Fried and Lin is also improper and should be withdrawn.

Independent claim 16 was also rejected based on Fried and Lin. Claim 16, as amended, is directed to a FinFET device comprising a number of features, including, for example, a gate material layer formed over a fin, a first sidewall spacer, and a second sidewall spacer, and in contact with the first and second sidewall spacers, in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers. Neither Fried nor Lin, either alone or in combination, disclose or suggest the gate material layer recited in claim 16.

As with claim 1, the Examiner contends that floating gates 115 of Fried correspond to Applicants' claimed first and second sidewall spacers and that gate 120 of Fried corresponds to Applicants' claimed gate material layer. (Office Action, page 9). As clearly shown and described by Fried, a floating gate isolation layer 116 is disposed between layers 115 and 120 of Fried. (see Fried, Figs. 8, 10, and 11, and column 5, line 39 through column 6, line 11). Thus,

floating gates 115 cannot be said to be in contact with gate 120. Accordingly, Fried does not disclose or suggest, as is recited in claim 16, a gate material layer formed over a fin, a first sidewall spacer, and a second sidewall spacer, and in contact with the first and second sidewall spacers, as recited in claim 16.

For at least these reasons, Applicants submit that Fried and Lin, either alone or in combination, do not disclose or suggest each feature of claim 16. Also, based on rationale similar to that given above with regard to claim 1, Applicants submit that the Examiner has not shown proper motivation to combine Fried and Lin in the manner suggested.

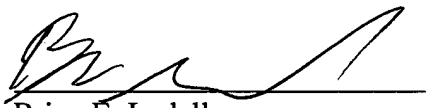
For at least these reasons, Applicants submit that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Fried and Lin is improper and should be withdrawn. At least by virtue of their dependency on claim 16, the rejection of claims 18 and 19 based on Fried and Lin is also improper and should be withdrawn.

In view of the foregoing amendments and remarks, Applicants submit that the claimed invention is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
Brian E. Ledell
Reg. No. 42,784

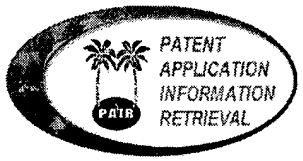
Date: April 27, 2005

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
Telephone: 571-432-0800
Facsimile: 571-432-0808
Customer Number: 45114

Attachment: PAIR printout of Assignment Page for An and Dakshina-Murthy

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL



PAIR
FAQ
Help
Feedback

Other Links

E-Business Center Patents
Employee Locator
Class/Subclass GAU Information
Information Contacts

Patent Assignment Abstract of Title

Total Assignments: 1

Application #: 10385652 **Filing Dt:** 03/12/2003 **Patent #:** 6800885 **Issue Dt:** 10/05/2004

PCT #: NONE **Publication #:** NONE **Pub Dt:**

Inventors: Judy Xilin An, Bin Yu

Title: ASYMMETRICAL DOUBLE GATE OR ALL-AROUND GATE MOSFET DEVICES AND METHODS FOR MAKING SAME

Assignment: 1

Reel/Frame:	Received:	Recorded:	Mailed:	Pages:
013870/0781	03/25/2003	03/12/2003	08/13/2003	3

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: AN, JUDY XILIN **Exec Dt:** 02/06/2003

YU, BIN **Exec Dt:** 02/06/2003

Assignee: ADVANCED MICRO DEVICES, INC.
ONE AMD PLACE
P.O. BOX 3453
SUNNYVALE, CALIFORNIA 94088-3453

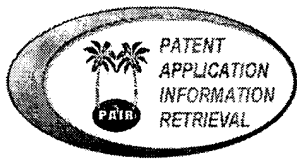
Correspondent: HARRITY & SNYDER, LLP
PAUL A. HARRITY
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

Search Results as of: 4/19/2005 10:04:40 A.M.

Disclaimer:
Assignment information on the assignment database reflects assignment documents that have been actually recorded.
If the assignment for a patent was not recorded, the name of the assignee on the patent application publication or patent may be different.
If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 703-308-9723

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL



PAIR
FAQ
Help
Feedback

Other Links

E-Business Center Patents
Employee Locator
Class/Subclass GAU Information
Information Contacts

Patent Assignment Abstract of Title

Total Assignments: 1

Application #: 10632989 **Filing Dt:** 08/04/2003 **Patent #:** 6787476 **Issue Dt:** 09/07/2004

PCT #: NONE **Publication #:** NONE **Pub Dt:**

Inventors: Srikanteswara Dakshina-Murthy, Cyrus E. Tabery, Chih-Yuh Yang, Bin Yu

Title: ETCH STOP LAYER FOR ETCHING FINFET GATE OVER A LARGE TOPOGRAPHY

Assignment: 1

Reel/Frame:	**Received:**	**Recorded:**	**Mailed:**	**Pages:**
014365/0305	08/13/2003	08/04/2003	02/25/2004	4

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors:		
DAKSHINA-MURTHY, SRIKANTESWARA	**Exec Dt:**	12/13/2002
TABERY, CYRUS E.	**Exec Dt:**	12/13/2002
YANG, CHIH-YUH	**Exec Dt:**	12/13/2002
YU, BIN	**Exec Dt:**	01/10/2003

Assignee: ADVANCED MICRO DEVICES, INC.
ONE AMD PLACE
P.O. BOX 3453
SUNNYVALE, CALIFORNIA 94088-3453

Correspondent: HARRITY & SNYDER, LLP
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

Search Results as of: 4/26/2005 4:16:37 P.M.

Disclaimer:
Assignment information on the assignment database reflects assignment documents that have been actually recorded.
If the assignment for a patent was not recorded, the name of the assignee on the patent application publication or patent may be different.
If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 703-308-9723